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FOR

CIRCUIT AND METHOD FOR A SWITCH MATRIX AND SWITCH SENSING

Inventor(s):

Kollin Tierling
622 Costigan Circle
Milpitas, CA 95035

Sawyer Law Group LLP
2465 E. Bayshore Road, Suite 406
Palo Alto, California 94303

CIRCUIT AND METHOD FOR A SWITCH MATRIX AND SWITCH SENSING

FIELD OF THE INVENTION

The present invention relates to a switch matrix, and more particularly to an efficient, low cost switch matrix.

BACKGROUND OF THE INVENTION

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In various interface devices, such as keypads, joysticks, wheels, gamepads, etc., detection of user selections of differing buttons and switches is needed. A standard switch matrix operates like a grid of horizontal and vertical conductors. At all points where the horizontal and vertical conductors cross, a switch is located. Pressing/closing the switch connects the two conductors. Figure 1 presents a functional diagram of a standard matrix 8 of sixteen (16) switches, a 4x4 matrix. In the standard 16 switch matrix, four of the conductors or row lines, Row 0, Row 1, Row 2, and Row 3, are dedicated to drive a voltage corresponding to a logic level zero into the matrix. Only one of the four rows is driven low

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at a time, and the remaining rows are passively pulled high by the pull-up resistors 10a, 10b,

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10c, or 10d on the top of the matrix. Four lines, Column 0, Column 1, Column 2, and Column 3, act as scan lines and are used to read back the state of the matrix. The row that is being scanned is the one that is at logic zero. The matrix is read by sampling the column conductors. For example, in the representation of Figure 1, closed switches are indicated by circles and open switches are indicated by a cluster of dots. Thus, one switch, switch 14bc, is shown as closed. When Row 1 is driven low during a scan of the matrix, Column 2 reads

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zero, which indicates to a processor 12 driving the rows and performing the scan that the switch 14bc corresponding to Row 1 and Column 2 is closed/pressed.

In certain situations, a problem with a switch falsely being interpreted as closed can arise. Figure 2 illustrates the closing/pressing of three switches, switch 14bb, switch 14cb, and switch 14cc, within the functional switch matrix diagram of Figure 1. Row 1 is driven low by the processor 12 in order to determine if any of the switches on Row 1 are pressed. Because switch 14bb is pressed, Column 1 is connected to Row 1 and Column 1 is forced low. The processor 12 then correctly detects that the switch 14bb at the intersection of Row 1 and Column 1 is pressed. Because Column 1 is low, and switch 14cb is also pressed, Row 2 is also connected to Row 1 through Column 1. This connection pulls Row 2 low. Since button switch 14cc on Row 2 is also pressed, Column 2 is likewise pulled low. Since the processor 12 is driving Row 1 low, it interprets the low on Column 2 as though the switch 14bc were closed, as indicated by the triangles in Figure 2. In this way, the switch 14bc is falsely interpreted as closed and is said to "ghost" the switch 14cc. In order to avoid such "ghosting", normally the design of a matrix solution must achieve the ability to properly identify closed switches while accounting for and overcoming the problem of "ghosting." In general, for the standard matrix diagram as shown in Figures 1 and 2, allowing only one of the scanning rows to be in the unique low state avoids the ghosting problem.

Figure 3 illustrates a conventional standard 4x4 switch matrix 20 for switch selection that avoids ghosting. As shown, there are 16 switches, S1 through S16, and 16 diodes, D1 through D16. The diodes act as one-way valves, which allow electrons to flow through the switches in only one direction, i.e., from higher voltage (logic 1) to lower voltage (logic 0) in a conventional circuit. The diodes further act to avoid a short circuit that could exist by

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pressing any two switches in the same column, which would draw too much current from the processor 12 driving the output lines.

The diodes in the standard switch matrix also act to overcome the ghosting problem. In the example of Figure 3, switch S6 is shown as closed. When ROW1 is driven low by the processor 22, diode D6 allows current to flow through S6, which pulls COL2 low. Note in the schematic, the diodes allow a row that is low (being scanned) to pull a column low. But, should a second switch be pressed within a column, such as switch S10, diode D10 prevents the low voltage on COL2 from pulling ROW2 low, since the diode D10 is reverse-biased (i.e., the side of the diode that the arrow is pointing to is at a higher voltage (+5V) thanthe opposite side of the diode (0V)). Since a reverse-biased diode will not conduct, only the row being driven low by the processor 22 will be low, and no other row will be pulled low, even if more than one switch in a column is pressed. In this manner, the ghosting problem, as described with reference to Figure 2, will not occur.

While the conventional switch matrix can provide switch selection indication and avoid ghosting, the conventional approach is input/output (I/O) intensive, requiring significant processor resources in providing scan line processing. The conventional switch matrix further requires one diode per switch to prevent ghosting, which adds considerable accumulative cost as the number of switches within a matrix grows. Accordingly, what is needed is a switch matrix that is more efficient and has a lower cost than the conventional switch matrix.

SUMMARY OF THE INVENTION

Aspects of a switch matrix circuit are provided. In accordance with a circuit aspect, a plurality of switches are organized in a row and column configuration. Coupled to the plurality of switches is a current sensing circuit. The current sensing circuit includes a transistor and at least one resistor per column of the plurality of switches. Current amplified by the transistor and converted by the at least one resistor in a column is sensed as a logic level indicative of a switch status within the column for a selected row.

Through the present invention, a more efficient and lower cost switch matrix circuit is provided. In one embodiment, the present invention senses current instead of voltage to detect open or closed switches, where resistors and a transistor are used for each column of the matrix to provide selection signals to a processor to determine which button(s) of the matrix have been pressed. In addition, the number of I/O lines going to the processor can be reduced by utilizing bi-directional scan lines and scanning only one switch at a time instead of an entire row of switches at a time. A further embodiment that is a variation on the current sensing matrix can use an analog-to-digital converter to sense the switch states, but, likewise, uses the bi-directional scan lines to reduce the number of I/O linens going to the processor. These and other advantages will become readily apparent from the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a functional diagram of a standard matrix of 16 switches.

Figure 2 illustrates the closing/pressing of three switches within the functional switch matrix diagram of Figure 1.

Figure 3 illustrates conventional standard 4x4 switch matrix that indicates switch selection while avoiding ghosting.

Figure 4 illustrates a schematic of a current sensing switch matrix in accordance with one embodiment of the present invention.

Figure 5 illustrates a voltage divider perspective of the circuit of Figure 4 where switches S10' and S6' are closed.

Figure 6 illustrates a second embodiment of the present invention that utilizes a single set of scan lines for input and output.

Figure 7 illustrates another embodiment of the present invention utilizing bi-directional scan lines.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to a switch matrix circuit. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Figure 4 illustrates a schematic of a current sensing switch matrix 100 in accordance with one embodiment of the present invention. As indicated by its name, the detection of a closed switch in the matrix is based on current. Similar to the conventional matrix, only one of the rows is driven low at a time. In the example of Figure 4, 16 switches, S1' through

S16', are included and each is coupled to one of 16 resistors, R1' through R16', (e.g., each 240Kohm) respectively. Further coupled to the switches S1' - S16' is a current sensing circuit that includes a transistor (Q1, Q2, Q3, and Q4, e.g., bipolar junction transistors), and at least one resistor (R17, R18, R19 (e.g., each 240Kohm), and R20, R21, R22, R23, and R24, (e.g., each 4.7Kohm)) for each column, Column_0, Column_1, Column_2, and Column_3, of the switch matrix.

To illustrate operation within the switch matrix of Figure 4, one switch, S6', is shown as closed. When Row_1 is driven low by a processor 20 coupled to the current sensing circuit, current flows through R6 and R18, as well as the base to emitter junction of Q2, which is the forward current path indicated by the arrow of Q2, as is well appreciated by those skilled in the art. Note that since only Row_1 is driven low, only the switches on Row_1 (S1', S2', S3', or S4') can switch on the transistors Q1 through Q4.

With the current flowing through the transistor Q2, the small base current is amplified into a large emitter to collector current. The emitter current is converted into a voltage by R22. Since the resistor R22 converts the current into a voltage, the current is sensed on Column_1 as logic 1 by the processor 120. The logic 1 on Column_1 indicates to the processor 20 that the switch S6', at the intersection of Row_1 and Column_1, is closed.

From a voltage divider perspective, if S10' were closed in addition to S6', then R10', R18, and R6' will form a voltage divider network as shown in Figure 5. Since R6' sees a drop of about 4.4V, it is conducting about 18.3 μA (microAmperes) of current. R10' and R18 each conduct only about 0.6V/240K = 2.5 μA. Accordingly, the balance of the current (18.3 -2.5 -2.5 = 13.3 μA) has to be flowing through the base of Q2, which still indicates that Q2 has been switched on and is sufficient to detect the closed switches when the

appropriate row for each switch is driven low. In fact, even if all four switches in Column_1 are closed, then the base of Q2 still has to be conducting about 8.3 μA, which is sufficient to turn on Q2 and pull Column_1 high to properly indicate the closed switches. Preventing ghosting with multiple switches closed occurs by applying the principle that no two rows

5   will be in the unique logic zero state simultaneously. Since the base to emitter junction of the transistor supplies ensures that the column will not drop below about 4.4V, i.e., no more than 0.6 V or so below the emitter or supply voltage of +5V in the example, even if switches S10' and S6' are both closed, for example, there will never be enough current through S10' to turn on any other transistors.

It should be noted that the term "processor" as used herein can refer to a variety of different types of controller circuits, such as microprocessors, microcontrollers, digital signal processors (DSP's), programmable logic arrays (PGA's), digital logic or state machines, etc.

Figure 6 illustrates a second embodiment of a switch matrix 200 of the present invention that utilizes a single set of scan lines (scan 0 - scan 4) for input and output. However, each scan line cannot be both an input and an output simultaneously. In order to support bi-directional scan lines, preferably the switches in the matrix are configured as rows and columns where the switch matrix has an off-set diagonal configuration of switches, so that there is a switch at each row and column intersection except for one intersection in each row, and the intersection lacking the switch lies in a different column among the rows.

20   Further, in order to maintain the principle that only one row can be in the unique logic low state, only one scan line is to be driven low by the processor 120 at a time, while one of the other scan lines acts an input line signal to the processor to read, and all other scan lines are driven high by the processor. For example, if switch S1 of row 0 is to be tested, scan line 0

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is driven low by the processor 120. In this case, scan line 1 acts as the input to processor 120 and the remaining scan lines 2 and 3 are driven high by the processor so that no current is passed through any other switches.
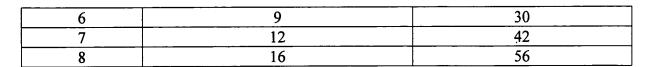
In this alternate embodiment, the use of bi-directional scan lines limits the scanning to only one switch at a time, instead of the conventional one row at a time. However, for a typical processor with a loop rate of 1 kHz (kiloHertz), the scanning of twenty switches is accomplished in about 20 ms (milliseconds), or one fiftieth of a second, i.e., the complete matrix can be scanned 50 times per second, which is sufficient for software debounce. Further, the utilization of the bi-directional scan lines realizes significant potential in saving cost.

In general, the number of switches that can be supported by a given number of I/O lines for a standard matrix is R + C, where R refers to the number of rows and C refers to the number of columns in the matrix. The number of switches in the matrix of the present invention grows in correspondence with S(S-1), where S refers to the number of scan lines. Notice that the number of switches supported by the conventional matrix grows roughly as $1/4 \ S^2$, whereas with the matrix of the present invention, the number grows as S^2-S. A shown by the following table, for a same number of I/O lines/pins, over three times the number of switches can be supported with the matrix in accordance with the present invention, as compared with the conventional matrix.

I/O LINES	STANDARD MATRIX SWTICHES	INVENTIVE MATRIX SWITCHES
1	1	1
2	1	2
3	2	6
4	4	12
5	6	20

6	9	30
7	12	42
8	16	56

Thus, a processor with fewer I/O lines can be used to support the same size or larger matrix than conventionally done, which allows for potential cost savings in the use of a smaller, cheaper processor. When used with the same size processor as in the conventional circuit,

5   the current sensing matrix can make available additional I/O lines that are no longer needed to support matrix scanning, thus allowing other features and value to be added to the product, as compared with an I/O intensive standard scan matrix. Of course, additional cost savings are achieved by eliminating the anti-ghosting diodes and replacing them with much lower cost resistors.

Figure 7 illustrates another embodiment of a switch matrix in accordance with the

10   present invention that also utilizes a single set of scan lines, SCAN1 through SCAN5, for input and output. Associated with each switch in the matrix is a resistor, e.g., a 10Kohm resistor, and associated with each scan line is a diode and resistor, e.g., a 100Kohm resistor. With this embodiment, a voltage sensing method is utilized, where a voltage threshold

15   sensing circuit 222 can be employed to sense voltage levels on the scan lines that correlate to unique switch states. The circuit 222 converts the voltage levels received from the switch circuit on the scan lines to logic states suitable for the processor 220, e.g. voltages above the set threshold are converted to a logic state of 1, and voltages below the threshold are a logic 0. Processor 220 is coupled to the circuit 222 by a signal bus 224. The circuit 222 can be an

20   analog to digital converter, for example. In one embodiment, the processor 220, the analog to digital converter 222 (for sensing voltages), and a general purpose input/output circuit (for allowing scanning of the scan lines) can all be included in a single package, such as a

ST7263 Microcontroller. In other embodiments, the components can be separate or other types of circuits can be used convert to logic states. For example, in a different embodiment, a voltage level converter including a transistor, as is known in the art, can be used on each scan line.

5   The voltage sensing matrix offers a lower cost implementation, since it replaces N transistors with N diodes (where N represents the number of scan lines), diodes being lower in cost than transistors. The constraints in determining the unique switch state include utilizing one of the scan lines as an analog input, driving one of the scan lines to a logic high level, and driving the remaining scan lines to logic low levels, where a processor, as described previously, performs the scan line driving.

           In sensing switch state in this embodiment, the switch that is being sensed is the one determined by the unique intersection of the row that is driven high and the column that is being sensed. For example, in the matrix shown in Figure 7, if SCAN1 through SCAN3 are at logic 0, SCAN4 is at logic 1, and SCAN5 is the input scan line, then switch S154, if closed, is the unique switch that could pull SCAN5 to a high logic level (+5V for 5V CMOS logic). While there may be the presence of other closed switches in the matrix, even if multiple switches are closed, there would still be sufficient ability to indicate a unique switch state. In general, with this embodiment, a unique switch is determined to be closed when the voltage on the input scan line exceeds one diode voltage level drop from logic 0

20   voltage level plus a small voltage allocation for noise margin. Additional noise margin could be added by using Schottkey diodes instead of standard small signal diodes, as is well appreciated by those skilled in the art.

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By way of example, if S151, S152, and S153 or any combination thereof are closed in addition to S154, then the voltage on SCAN4 will be in the range of 1.24V to 5V, depending on the number of the switches S151 through S153 that are additionally closed. If switches S115, S125, S135, S141, S142 and S143 are also closed, then the voltage on SCAN5 would be at least 1.09 volts, which is still higher than a silicon diode nominal forward voltage drop of 0.7V, and thus, would still sufficiently indicate a high logic level for a closed switch. Thus, in this example, the threshold used for high and low logic states is about 1.0 to 1.1 volts.

The resistors R101 through R105 are a practical addition to the matrix for applications where the controlling device has leakage currents that could adversely affect the voltage level on the input scan line. The diodes D101 through D105 ensure that the unique switch determined by the intersection of the logic one scan line row and the sense line column can bring the input scan line to a voltage level that exceeds one diode drop above logic 0. If the diodes were not present and the line shorted, then a second switch determined by the intersection of the column driven high and the input sense line row could also pull the sense line to a voltage that is higher than one diode drop from logic 0. Thus, none of the switches except for the unique switch described above can apply a voltage to the input scan line, and no combination of switches is likewise able to apply a voltage to the sense line that exceeds one diode drop from the logic 0 voltage level of the scan lines that are configured as logic 0. This provides anti-ghosting for the matrix.

Alternatively, the matrix could be arranged more as a half-matrix, such that only the upper (i.e., switches S121, 131, 141, 151, 132, 142, 152, 143, 153, 154) or lower (i.e., switches S112, 113, 123, 114, 124, 134, 115, 125, 135, 145) off-diagonal set of switches is

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populated. In this arrangement, the diodes would no longer be required, since the closed

switch that is pulling the input scan line above one diode drop from logic 0 would be unique.

A half-matrix arrangement could also be utilized with the above-described current sensing

embodiment to eliminate the need to use transistors. While the half-matrix arrangement

5   does reduce the number of switches being sensed, the total number still exceeds what could

be supported in the prior art arrangement. For example, when N=5, as is Figure 7, a switch

matrix of one of the above embodiments with active components supports 20 switches

versus 10 switches for the half matrix without active components. In contrast, a standard

switch matrix would only support 6 switches.

Another alternate can be achieved by inverting the logic sense of all driven and

sensed lines and reversing the diode direction, if included. In this variation, the valid voltage

level that indicates "closed" is any voltage level above 0 volts plus allocation for noise

margin. There is similarly a symmetrical inverse design for the current sensing matrix.

From the foregoing, it will be observed that numerous variations and modifications

15   may be effected without departing from the spirit and scope of the novel concept of the

invention. It is to be understood that no limitation with respect to the specific methods and

apparatus illustrated herein is intended or should be inferred. For example, the switch

matrix of the present invention can be used in a wide variety of interface or electronic

devices, including keyboards, joysticks, gamepads, steering wheels, cellular phones, PDA's,

20   electronic appliances, or any device having multiple electrical switches or buttons. The

processor controlling the scanning can be integral to the device having the switches, or be

located across a physical or wireless bus. It is, of course, intended to cover by the appended

claims all such modifications as fall within the scope of the claims.